A low-power optoelectronic memory device based on MoS_2/BN/graphene heterostructure

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Abstract: A low-power optoelectronic memory device is demonstrated by charge trapping in a MoS_2/BN/graphene van der Waals heterostructure. The miniaturized structure, large current switching ratio (~6×10^5) and fast read/write speed (50 ms) suggest its potential in integrated non-volatile storage cell. © 2019 The Author(s)

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1. Introduction

Memory or information storage devices are important components of modern digital systems and integrated circuits. Traditional silicon-based electronic devices typically suffer from short channel and power dissipation issues. The atomically-thin nature and large heat extraction coefficient of two-dimensional (2D) materials allow fabricating nanoscale transistors for highly integrated systems, and may become essential building blocks for next-generation low-power electronic and optoelectronic devices. The ease with which to tune the carrier concentration of the low dimensional materials has enabled large ON/OFF ratio, which is a key figure-of-merit for non-volatile memory devices. In addition, high mechanical strength and robust electrical performance suggest 2D heterostructure's applicability in flexible and wearable devices.

While several 2D materials-based memories, such as graphene, WSe_2 and BP, have been developed, [1-4] the memory window or ON/OFF current ratio is small. Recently, an optoelectronic memory device based on a WSe_2/BN heterostructure is demonstrated to possess a large switching ratio (~10^6). However, the storage data is probably lost after power off, and the relatively large applied voltage in read/write process compromises its power consumption. [3,5-6]. Here we report a low-power optoelectronic memory based on MoS_2/BN/graphene heterostructure, in which boron nitride (BN) and graphene are employed as the charge barrier and trapping layer, respectively. Benefiting from the excellent carrier storage capacity of the fewer-layer graphene, a large electrical hysteresis window and a high current switching ratio (~6×10^5) are obtained. Especially, the photo-induced doping for MoS_2 channel allows optoelectronic operation with a ~10^3 current ratio at zero gate bias. The weak OFF-state current suggests a low static power dissipation (~0.2 nW).

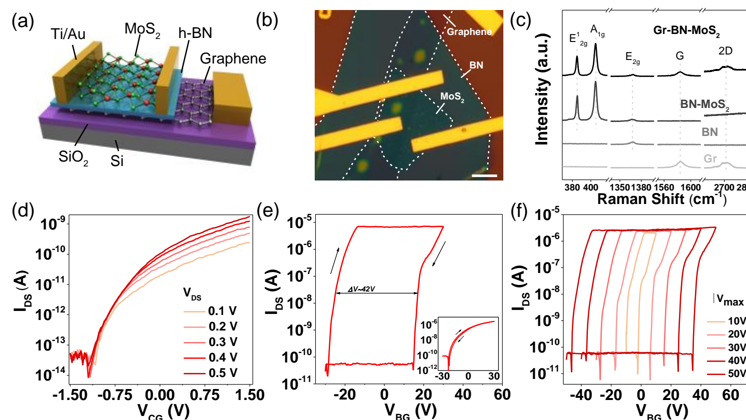

Figure.1 (a) Schematic of the memory device. (b) Optical microscope image of the device. The scale is 5 μm. (c) Raman spectra of each constituent material and the heterojunction region. (d) Transfer curves of the MoS_2 using the graphene as the gate. (e) Hysteresis of the transfer curve. Inset: the transfer curve of the MoS_2/BN/SiO_2 without graphene. (f) Hysteresis characteristic curves acquired from different sweeping voltage ranges.

2. Device fabrication and electrical characterization

Figure 1a shows the structure of the floating gate heterostructure memory. The graphene flake was deposited onto SiO_2/Si substrate through mechanical exfoliation. Then few-layer BN, MoS_2 flakes were placed over the graphene by dry transferring processes. The electrodes (7nm/80nm Ti/Au) were patterned by electron beam lithography and electron beam evaporation. Figure 1b shows the microscope image of the device. The typical Raman signatures of

graphene (G peak at 1583 cm^{-1} and 2D peak at 2714 cm^{-1}), BN (E_{2g} peak at 1367 cm^{-1}) and MoS_2(E^1_{2g} peak at 385 $cm^{-1}$and A_{1g} peak at 405 cm^{-1}) are observed (Fig. 1c).

Electrical characterizations were carried out in vacuum at room temperature. The transfer curves of the MoS_2 flake using graphene as gate (V_{CG}) electrode suggest a well modulation of the channel carrier concentration (Fig. 1d). Figure 1e shows the hysteresis loop of the transfer curve (from -30V to +30V then return to -30V). Memory window (defined from the shift of threshold voltage) can reach up to ~42 V, implying great information storage ability. Control experiment without graphene eliminates the influence of surface states in the interface of MoS_2/BN (inset of Fig. 1e). In addition, the memory window can be modulated by the sweeping gate voltage range, and it can exceed 80 V, when sweeping back gate bias within ±50 V (Fig. 1f).

3. Working mechanism and reliability test

The working mechanism can be explained by a simple energy band diagram in Fig. 2a. As the back gate voltage is swept toward positive value, electrons in MoS_2 are transferred into graphene layer by Fowler-Nordheim tunneling with the assistance of gate electric field [7, 8]. The accumulated negative charges in graphene induce a positive shift of the threshold voltage (erase state). By contrast, when reversed sweeping voltage is applied, holes are transferred to the floating gate and recombine with the accumulated electrons (program state).

The reliability of device operation is confirmed by robust and reproducible switching behavior (Fig. 2b, c). The information is read by measuring the source-drain current at V_{BG}=0V. For this purpose, low current ("0"), high current ("1") represent erase and program state, respectively. The gate pulse (±30 V, 50 ms) can realize a rapid electrical read/write operation with ~6×10^5 ON/OFF ratio, as shown in Fig. 2b. Interestingly, the strong light-matter interaction and photo-induced charge transferring process allow the photon writing operations (Fig.2c, 405 nm, 41.3 μW), suggesting an optical memory with a 10^3 ON/OFF ratio. More significantly, the storage state is unchanged after power off, suggesting a low static power consumption of ~0.2 nW (calculated by V_{DS}=2 V and I_{DS}= 10^{-10} A in erase state) and non-volatile information storage.

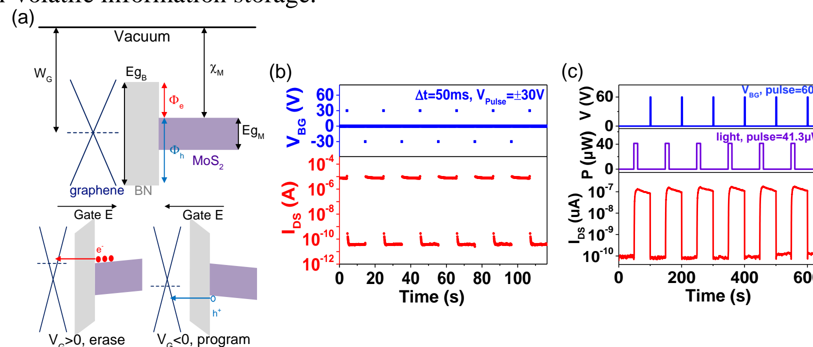

Figure.2 (a) Band diagrams of the memory for initial, program and erase states. (b) Switching behavior upon applying alternating V_{BG} pulse of ±30V. (c) The dynamic response for photon writing (high current) and electrical erasing (low current) states.

4. Conclusion

We have demonstrated a low-power non-volatile optoelectronic memory device based on a MoS_2/BN/graphene heterostructure. Rapid electrical and optical information read/write operation and high switching radio are successfully achieved. Such a miniaturized device paves the way for developing novel optoelectronic storage cell with ultra-low power consumption and high integration.

5. References

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